REMARKS/ARGUMENTS

These remarks are filed in response to the Examiner's Report of May 17, 2005. The applicant hereby petitions for a one-month extension of time to the deadline for filing the present response to Office Action. With a one-month extension of time, the deadline for filing this response is September 17, 2005. A Fee Transmittal Form is enclosed herewith authorizing the Commissioner to deduct the requisite fee under 37 C.F.R. 1.17(a)(1) from Deposit Account No. 13-2400. The Commissioner is hereby authorized in this and subsequent replies to deduct any fees or credit any overpayments to Deposit Account No. 13-2400 for any additional fees required under 37 C.F.R. 1.16 or 1.17; particularly, extension of time fees.

These remarks are also being filed concurrently with an Information Disclosure Statement.

In the Office Action of May 17, 2005, the Examiner rejected claims 1, 2, 4, 5, 7, 10-13, and 15 under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,885,828 (Cornelius). The Examiner also rejected claims 8, 17, 18 and 20 as being obvious having regard to Cornelius in view of US Patent No. 5,455,536 (Kono et al.). Claims 3, 6, and 14 were rejected as being obvious having regard to Cornelius in view of US Patent No. 6,583,903 (Way et al.) and claim 16 was rejected as being obvious having regard to Cornelius in view of US Patent Publication No. US2003/0120799 (Lahav et al.). The applicant has carefully considered the Examiner's rejections, but traverses those rejections for the reasons that follow.

In rejecting independent claims 1 and 11 as being anticipated by the Cornelius reference, the Examiner cites the passages at column 5, lines 57-67 and page 6, lines 1-26, as teaching a step or performance monitor for comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic "1"s and logic "0"s that have been corrected by the error corrector. A careful review of the Cornelius reference reveals no such teaching.

Cornelius teaches an optical receiver configuration and method of controlling an optical signal receiver that adjusts a decision threshold based upon a total percentage error indicator. The total percentage error indicator is used to variably adjust the decision threshold used for analog to digital conversion. In particular, Cornelius suggests that a comparator reconstructs a digital electrical signal from an input analog signal and the reconstructed digital electrical signal is provided to a clock data recovery circuit 18. The clock data recovery circuit outputs a clock signal to an error detection and correction circuit 20. The error detection and correction circuit 20 also receives the digital data signal. As noted at the passage referred to by the Examiner, the error detection and correction circuit 20 outputs an error signal on line 36. The error signal is representative of the number of errors received in the input data stream. The error signal preferably conveys the number of corrected "1"s and the number of corrected "0"s. The error detection circuit 20 also outputs a corrected data output on line 46.

As shown in the figures, such as Figure 2, the error detection and correction circuit 20 receives the input data stream and outputs a corrected data stream. The error detection and correction circuit 20 also outputs the error signal 36. Nowhere does Cornelius teach or suggest a performance monitor that receives both a corrected data signal and an uncorrected data signal and compares the signals to determine the relative number of logic "1"s and logic "0"s that have been corrected. Since the independent claims in the present application (claims 1, 11, and 17) each specify that the method or system involves a comparison between the uncorrected binary data signal and the corrected binary signal to determine the relative number of logic "1"s and logic "0"s corrected, the applicant respectfully submits that the Cornelius reference cannot be considered anticipatory under 35 U.S.C. 102(e), and respectfully requests that the Examiner withdraw this rejection.

In rejecting independent claim 17, the Examiner acknowledged that Cornelius failed to teach a bit-by-bit comparison of the corrected and uncorrected binary data signals. The Examiner alleged that it would have been obvious to combine the teachings of Cornelius with the teachings of the Kono et al. reference in order to arrive at the device claimed in claim 17.

The Kono et al. reference describes a demodulator circuit. The demodulator circuit includes an error corrector that performs error correction upon an input receive data signal and produces corrected data. A comparator compares the corrected data with the uncorrected data to produce an output pulse when the two signals are not coincident with each other. This pulse is provided to an error counter that increments an error count each time a pulse is received.

The Examiner has alleged that it would be obvious to combine the Cornelius reference with the Kono et al. reference to arrive at the system or method claimed in the present application. In the applicant's respectful submission, one of ordinary skill in the art would not combine these two references in the manner suggested by the Examiner. The Kono et al. reference teaches a monitor for tracking the bit error rate in a received signal. In particular, the monitor compares a corrected and uncorrected version of the bit stream and counts, in absolute terms, the total number of errors corrected on a bit-by-bit basis. Kono et al. fails to teach or suggest determining the number of logic "1"s corrected to logic "0"s as compared to the number of logic "0"s corrected to logic "1"s. Accordingly, the Kono et al. reference fails to teach tracking the relative number of corrected logic "1"s and logic "0"s. Without knowledge regarding the relative number of logic "1"s and "0"s, the system and method cannot determine the manner in which to adjust the threshold level in an analog-to-digital converter. Accordingly, the applicant respectfully submits that one of ordinary skill in the art would not be inclined to combine the teachings of the Kono et al. reference with the teachings in Cornelius.

Moreover, even if one were to combine the Cornelius reference with the teachings of Kono et al., one does not arrive at the present invention. If the bit error monitor of Kono et al. were employed to implement a portion of the error detection and correction circuit 20 described in Cornelius, the error signal output on line 36 would be a total count of the number of errors corrected in the input data stream.

Claim 1 of the present application specifies a performance monitor for comparing the corrected binary data signal with an uncorrected representation of the binary data

signal to determine information about the relative number of logic "1"s and logic "0"s that have been corrected by the error corrector and output a feedback signal representative of said information. Claim 11 of the present application specifies a method for regenerating a binary data signal, including a step of comparing the corrected binary data signal with an uncorrected representation of the binary data signal to determine information about the relative number of logic "1"s and logic "0"s that have been corrected. Claim 17 of the present application specifies performance monitoring device comprising comparison means for receiving a corrected binary data signal and an uncorrected binary data signal from the data regenerator and performing a bit-by-bit comparison of the corrected and uncorrected binary data signals to determine when a logic "1" has been corrected to a logic "0" and when a logic "0" has been corrected to a logic "1" by the data regenerator, and signal generating means responsive to the comparison means for generating an output representative of the relative number of corrected logic "1"s and logic "0"s. Accordingly, each of the independent claims of the present application specify a system, method, or device that determines and responds to the relative number of corrected logic "1"s and logic "0"s. Because the Kono et al. reference teaches only a system for tracking the total number of corrected bits, a person of ordinary skill in the art would not arrive at the present invention through combining the teachings of Kono et al. with the system described in Cornelius. Therefore, in the applicant's respectful submission, the present application is patentably distinguishable over Cornelius in view of Kono et al., and the applicant respectfully requests that the Examiner withdraw this rejection.

The additional art cited by the Examiner, including Way et al. and Lahav et al. fails to correct the deficiencies in the teachings of Cornelius and/or Kono et al. Accordingly, the applicant respectfully submits that the present claims are patentably distinguishable over Cornelius in view of Way et al. and/or Lahav et al.

In view of the foregoing comments, the applicant respectfully requests that the Examiner withdraw her art-based rejection of claims 1-8, 10-18, and 20, and requests that a timely Notice of Allowance be issued.

Should the Examiner be minded to reject the applicant's submissions and maintain the current rejections, the applicant respectfully requests a telephone conference so as to expedite prosecution. The Examiner can reach the applicant's agent, Fraser Rowand, at (416) 868-1482.

Respectfully Submitted,
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